High-Rate Ka-Band Modulator for the NISAR Mission

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***Abstract*—In order to meet ever-increasing data return requirements, more satellites are using the near-Earth Ka-band (25.5 – 27.0 GHz) to achieve higher downlink rates. The paper discusses the Universal Space Transponder - Ka-band Modulator (UST-KaM) developed at the NASA Jet Propulsion Laboratory for the NASA-ISRO SAR (NISAR) mission, which is capable of transmitting up to 1.74 Gbps with 7/8 LDPC encoding. The UST-KaM utilizes OQPSK with both baseband and RF filtering to contain the 1 Gsps transmission spectrum within the 1.5 GHz Ka-band, even with the use of an external, saturated amplifier. Due to the high data rates involved, several technical hurdles were overcome in both the digital and RF designs. The UST-KaM is a software defined radio with two digital circuit board assemblies: a low speed housekeeper board for commanding and telemetry, and a high-rate signal processing board known as the Signal Processing Module (SPM). The SPM receives data from the spacecraft via a SERDES interface at up to 2 Gbps, processes and encodes the data using a Xilinx Virtex-5 FPGA, and produces 1 Gsps OQPSK I and Q waveforms via synchronized, multiplexed DACs. The RF Electronics in the UST-KaM employ a heterodyne architecture in which the I/Q digital waveforms are filtered and then up-converted using a sub-harmonic IQ mixer. The LO of the converter, which is included in the exciter assembly, is at 13.125GHz, and the RF output is a 26.25GHz carrier which is modulated with the OQPSK waveforms. The output of the mixer is then filtered using low loss quartz thin-film edge coupled Chebyshev filters and amplified through a series of low gain Ka-Band amplifiers. The exciter assembly also has a 2GHz, low-phase-noise, PLL synthesizer to supply the clock to the DACs for the high rate digital waveforms.**

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1. INTRODUCTION

The NASA-ISRO Synthetic Aperture Radar (NISAR) mission is a joint effort between NASA and the Indian Space Research Organisation (ISRO) to launch an Earth-orbiting satellite with a dual-band synthetic aperture radar (SAR). Using both a NASA/JPL-provided L-band SAR and an ISRO-provided S-band SAR, the satellite will provide data collection of solid earth deformation, ice masses, and the ecosystem (biomass vegetation levels and the carbon cycle) in order to determine quantitatively the overall Earth change in unprecedented detail. The radars employ a SweepSAR technique via a 12 m reflector to obtain a wide swath (> 240 km) for global data collection via a repeat orbit of 12 days in length. In order to provide this extensive science coverage, the NISAR observatory will collect an average of 26 Terabits of science per day. A major challenge of the mission is downlinking this immense data volume.

During the mission formulation, it was determined that operating two circular polarized channels in the near-Earth Ka-band (25.5 – 27.0 GHz) was necessary to handle the ~3.5 Gbps downlink rate desired for the science data return [1]. In 2014, an assessment of commercially available Ka-band flight transmitters found none capable of >1 Gbps with the NASA Technology Readiness Level (TRL) needed for the project to proceed to the final design and fabrication phase. This lead to a JPL internal development of the Universal Space Transponder – Ka-band Modulator (UST-KaM) with the goal of enabling new greater data return volumes for both NISAR and other future near-Earth missions. An engineering model (EM) of the UST-KaM was built and underwent laboratory and environmental testing to demonstrate TRL6. Key specification of the radio are shown in Table 1.

This paper discusses the development of the UST-KaM, providing an overview of the unit architecture and the rationale behind it, as well as design details and the challenges of achieving such high data rates. Additionally, TRL6 test details and results are presented, followed by the status of the assembly of flight models for the NISAR mission and discussion of the future plans for the UST-KaM.

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Table 1 - UST-KaM Key Specifications

TX Specs	
Frequencies	Ka-band (25.5-27 GHz)
Bandwidth	< 1.5 GHz
Coded Data Rates	500, 1000, 2000 Msps
Modulations	QPSK / OQPSK with Custom Baseband Analog Filtering
Digital Pulse Shaping	Root Raised Cosine (Optional)
Channel Coding	LDPC with Rate 223/255 (~7/8)
RF Output Power	+12 dBm
Interface Specs	
Mass	4.5 kg
Power Consumption	40 W TX Mode 20 W Standby Mode
Cmd/Tlm Interface	1553, RS-422, or Spacewire
High Speed Data Interface	TLK WizardLink SERDES (up to 2 Gbps)
Power Interface	22-36 V Unregulated Bus
Dimensions	25 x 20 x 11 cm (L x W x H)
Environmental Specs	
Flight Allowable Temperatures	-20° to +50° C
Mechanical Environments	>15 grms Random Vibration >2000 g Shock
Radiation	50 krad

2. ARCHITECTURE

Modulation and Encoding

The UST-KaM was designed with the primary goal to utilize the entire near-Earth Ka-band to provide the maximum downlink rate in an SNR efficient manner. However, the transmission needs to stay in compliance with the National Telecommunications and Information Administration (NTIA) spectral mask for the 1.5 GHz band allocation, as well as the Space Frequency Coordination Group (SFCG) Rec 21-2R3 emissions mask. Because of uncertainty in the RF amplifier that would be used with the UST-KaM, it was also desired to minimize spectral regrowth due to a saturated external amplifier.

Offset-QPSK (OPSK) was selected as the best modulation option to meet the design goals. While not as bandwidth efficient as higher order modulations, such as 8-PSK or 16-APSK, OQPSK offers the best Eb/No performance, reducing the required link SNR. The offset I and Q transitions also makes OQPSK uniquely resilient to spectral regrowth by saturated amplifiers, even after significant filtering. This allowed for more aggressive filtering at baseband, which offers much better passband performance and filter roll off for such a wideband signal.

Previous studies have demonstrated that OQPSK can be filtered with a single-sided bandwidth as low as half the bit rate and experience limited spectral regrowth [2]. For the UST-KaM, this lead to 1 GHz low-pass filters on the I and Q waveforms prior to modulation. MATLAB simulations demonstrated that this filtering provided sufficient rejection of the side lobes to comply with the NTIA and SFCG emission masks, even after a fully saturated RF amplifier (see Figure 1). The use of Root Raised Cosine (RRC) digital pulse shaping is capable of further constraining the transmit spectrum and possibly reducing distortion noise, depending on the saturation level of the external amplifier. The UST-KaM is optionally able to provide RRC pulse shaping with two samples per symbol for mission scenarios where this is beneficial.

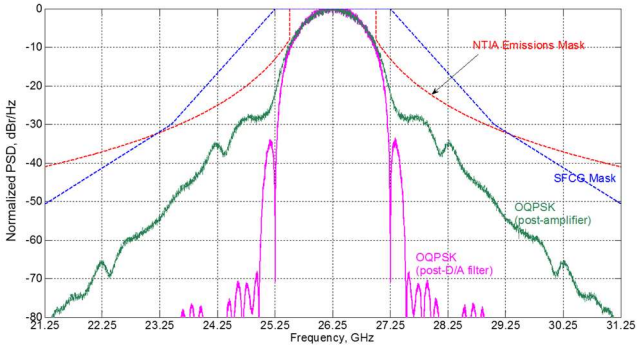

Figure 1 - Simulated Spectrum of Baseband-Filtered OQPSK pre and post Saturated Amplifier

The (8160,7136) low-density parity-check (LDPC) code from the Consultative Committee for Space Data Systems (CCSDS), commonly referred to as LDPC 7/8, was selected as a forward error correction coding for the UST-KaM. This high-rate code minimizes the reduction in data throughput, while still offering significant link performance improvement. At a bit error rate of 1e-8, this LDPC coding provides 8 dB of coding gain. It is also designed to integrate with the CCSDS Advanced Orbiting Systems (AOS) communication protocol, sharing a single Attached Sync Marker (ASM) and reducing framing overhead. To ensure that the transmit waveform has sufficient bit transition density regardless of the data source, the UST-KaM employs a length-255 pseudo-randomizer. This randomizer is

designed for easier implementation with the LDPC 7/8 encoding. Importantly, this modulation and encoding approach is compliant with the CCSDS Recommendation for Space Data System Standards (CCSDS 131.0-B-2) and compatible with NASA's Near-Earth Network, which the NISAR mission will be using as ground stations.

Hardware Architecture

The UST-KaM was developed within JPL's Universal Space Transponder (UST) radio product line. The UST is a next generation transponder developed at JPL to meet a large variety of telecom, navigation, and radio science needs for future deep-space and near-Earth missions [3]. The UST uses a modular hardware architecture, where custom RF modules are stacked on top of two core models: the Digital Processor Module (DPM) and the Power Supply Module (PSM). The DPM provides digital interfaces with the spacecraft, handles unit housekeeping functions, and provides baseband processing for any transmit or receive signals, and the PSM provides regulated secondary voltages and a 50 MHz reference for the other modules. Utilizing this common UST architecture for the UST-KaM simplified development and provides the benefit of in-flight reprogrammability of the application software and modem processor firmware.

In order to support the high data rates required, the signal processing board in the DPM needed to be customized for the UST-KaM. A typical UST can support multiple RF link simultaneously, but for the UST-KaM, the unit is tailored to support a single 2 Gbps transmission. This required a customized high-speed Serializer/Deserializer (SERDES) interface with the spacecraft, up to 16 bit parallelization in the modem processor FPGA, and two high-speed, multiplexing DACs that are sample synchronized.

A custom Ka-band RF transmit module (KTM) was also developed. The KTM provides the baseband I/Q filtering and wideband modulation directly at 26.25 GHz, and it also produces a 2 GHz reference for the DACs in the DPM. A functional diagram of the different UST-KaM modules and their interfaces is shown in Figure 2.

3. DESIGN

Digital Processor Module

The core of the UST-KaM is the DPM, an in-flight reprogrammable slice, which offers digital encoding and modulation functions, manages interfaces with the spacecraft avionics, and implements overall unit control. The DPM consists of two circuit board assemblies – the General Processor Board and the Signal Processor Board – that communicate over two board-to-board connectors. A high-level functional diagram of the DPM is shown in Figure 3.

To achieve the software-defined-radio (SDR) architecture, the DPM incorporates two key reconfigurable elements: a Payload Controller (PC) based on a radiation-hardened 32-bit SPARC V8 Microprocessor and a Modem Processor (MP),

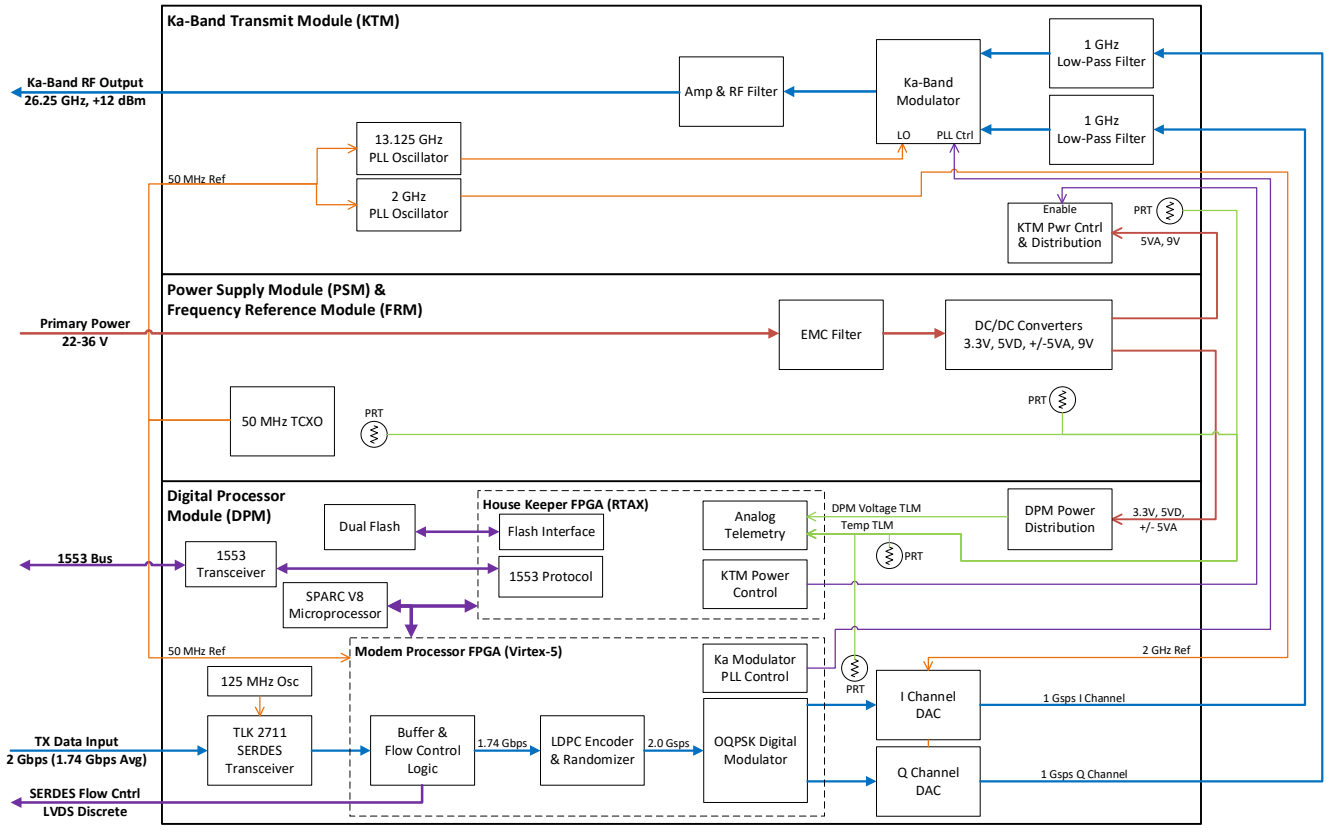

Figure 2 - UST-KaM Functional Diagram

which is implemented using a radiation-hardened space-grade Xilinx Virtex-5 reprogrammable FPGA. In addition, the DPM includes a Housekeeper (HK), which is a radiation-tolerant one-time programmable Actel/Microsemi RTAX-S FPGA, along with a substantial amount of dynamic and static memory.

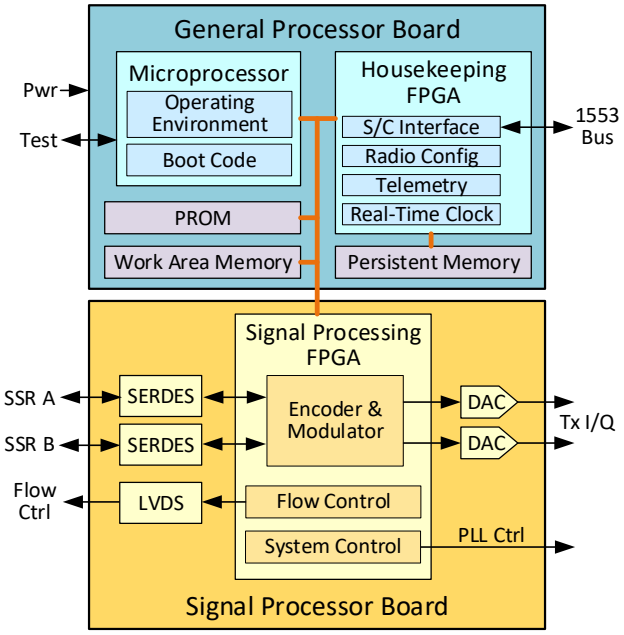

Figure 3 - Digital Processor Module Functional Diagram

The DPM handles the spacecraft interfaces, which include a MIL-STD-1553B interface, SpaceWire, discrete controls, and a high-speed data input. The 1553 is managed by the PC with the protocol logic housed inside of the HK FPGA interfacing with an industry-standard dedicated 1553 transceiver IC. The 1553 interface is the primary command and low-rate telemetry interface to the host spacecraft. In addition to the 1553 interface, the DPM also supports higher rate spacecraft command and telemetry interfaces, including SpaceWire over LVDS or RS-422 based serial protocols, which allows for speeds up to 200 Mbps. Three available optocoupler discrete inputs to the DPM could be used to receive direct commands from the spacecraft, such as Power-On Reset (POR) or a variety of other synchronization signals that may be required. A high-rate data input interface with the Solid State Recorder (SSR) is achieved via the MP PFGA interfacing to two TI TLK2711 SERDES transceivers. The DPM allows for dual-channel redundant SERDES interfaces supporting burst rates up to 2 Gbps. An LVDS flow-control line to the SSR is also available to facilitate handshaking and add robustness to the SSR to DPM data interface.

The other side of the DPM handles the interfaces to other slices of the radio stack, including controls for the Power Supply Module (PSM) and the RF module. The Housekeeper FPGA provides the primary means for control and management of telemetry signals to and from the UST-KaM front-end, and the Modem Processor (MP) FPGA encodes and digitally modulates data from the SSR and provides I/Q channels out to the KTM slice. The DPM also provides a suite of differential and single-ended general purpose or spare inputs and outputs that are not being utilized in the existing design, but provide means for growth to meet future mission requirements while minimize cost and schedule associated with NRE.

For operation in the long-term spaceflight environment, the DPM has several layers of built-in protection from radiation-induced SEUs. The design features EDAC protection on all internal and external FPGA memory interfaces. The DPM also includes a periodic "scrubbing" functionality that autonomously corrects any SEUs in the MP FPGA configuration without interrupting its current operation. The use of one-time programmable components, such as software boot PROM and HK FPGA, further ensures that the UST-KaM can maintain basic functionality and reprogrammability for recovery, even in the face of severe SEU activity.

Photos of the DPM are shown in Figure 4 and Figure 5 with key components labeled.

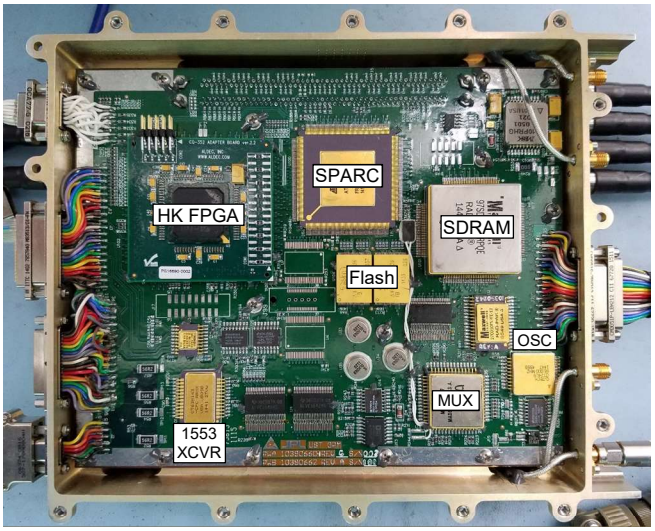

Figure 4 - EM DPM Slice Top

The Modem Processor employs a register based Payload Controller interface, which allows for real-time reconfiguration of various features of the FPGA. The MP is responsible for receiving the SSR data, encoding and modulating it, filtering the modulated I and Q symbols, and feeding them to the high-speed Digital to Analog Converters (DACs). The MP consists of multiple interfaces and modules that orchestrate this task. Given that the data needs to be transmitted at rates up to 2 Gbps, a serial data processing scheme was ruled out in favor of a parallel data processing implementation. Unique FPGA encoding and modulation designs were developed to allow the processing to run at a rate 16 times slower than 2 GHz and still support the 2 Gbps encoded data throughput. A functional diagram of the MP is shown in Figure 6.

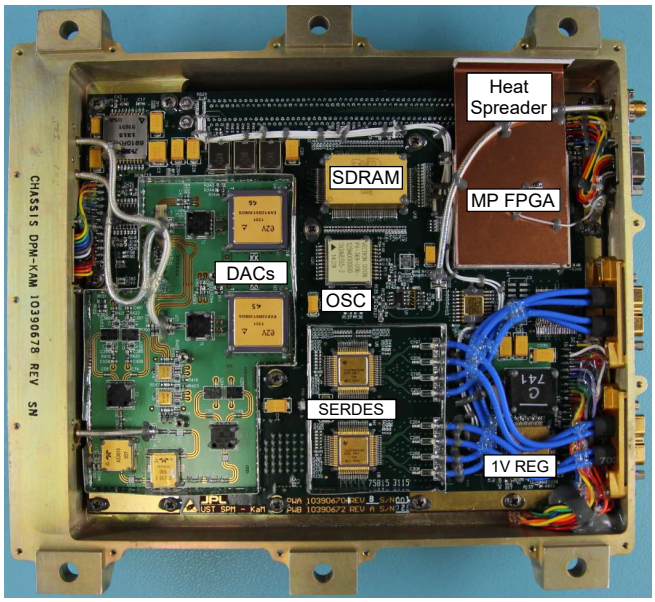

Figure 5 - EM DPM Slice Bottom

SSR Interface—The FPGA receives transmit data from the SSR via a SERDES data link provided by TLK2711 transceivers on both ends. The SSR transmits data via its TLK2711, which performs 8b/10b encoding and transmits the encoded data at 2.5 Gbps (effective 2 Gbps raw data rate). The SPM receives the serial data, decodes it, and provides it to the MP FPGA as 16-bit parallel data at a 125 MHz clock rate. The FPGA receives the data and stores it in one of the four internal FIFO buffers. Each buffer is large enough to store a complete 7136-bit long AOS frame of data before feeding it to the encoder. The SSR interface includes logic to determine whether an incoming frame is valid. All invalid data will be discarded.

Flow control is provided via an LVDS discrete, which tells the SSR to stop sending data when asserted. The buffer is sized and flow control asserted based on the assumption that the SSR responds to the flow control signal within a number of 125 MHz clock cycles, although there is significant flexibility in the FPGA design (it can actually accommodate several hundred clock cycles of latency). The received data is encoded with a LDPC rate 7/8 encoder, which takes in data at 1.74 Gbps and outputs coded data at 2 Gbps. Thus, the average data rate of the SSR SERDES link is 1.74 Gbps (2 Gbps data rate with flow control asserted ~13% of the time).

Redundant SSR interfaces are provided, each with its own FPGA logic and TLK2711 & LVDS transceivers. The A and B interfaces can be selected via an FPGA register bit. Only one interface can provide data to the transmitter processing path (encoder + modulator) at a time, but the two interfaces can be used simultaneously in test mode.

Word alignment is achieved by the TLK2711 via a specific sync pattern ([K28.5 D5.6] [K28.5 D5.6]), which the SSR transmits whenever it is idle (flow control asserted). The MP FPGA provides a count of sync patterns detected as status of the "aliveness" of the SSR and SERDES link. The FPGA also detects several error conditions reported by the TLK2711 (e.g. decode errors, loss-of-signal) and provides telemetry as further status as to the health of the SERDES link.

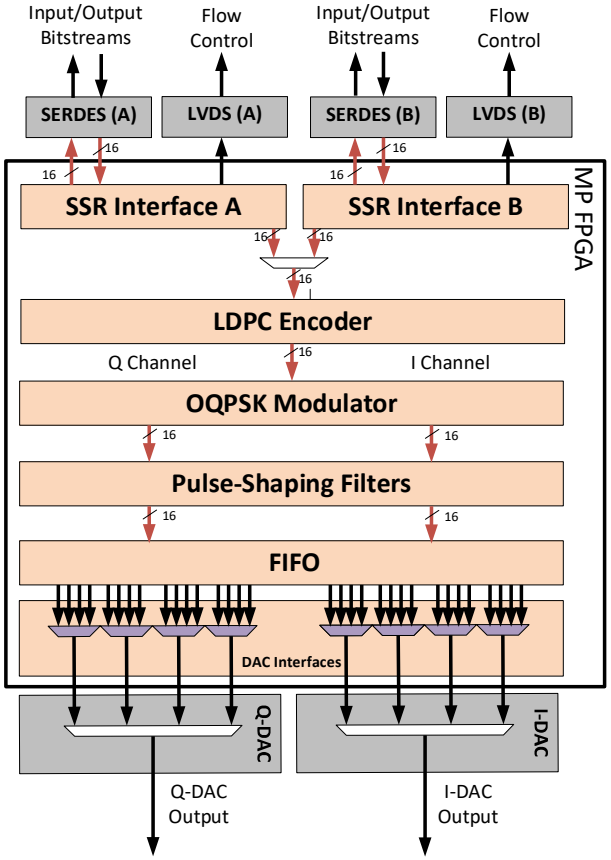

Figure 6 - MP Functional Block Diagram

In addition to the nominal operation, several test modes are also provided to help verify proper behavior of the SSR interface.

- The TLK2711 internal loopback mode can be enabled to loop back any data presented on the parallel transmit interface directly into the parallel receive interface. This mode allows the TLK2711 to FPGA interface to be verified without the use of the serial interface.
- The TLK2711 pseudo-random bit stream (PRBS) mode can be enabled to verify the serial side of the SERDES interface. If this mode is enabled on both SERDES connected in a loopback configuration via an external cable, the FPGA will detect bit errors as reported by the receiving TLK2711 as described in the datasheet. This mode allows the TLK2711 serial interface to be verified in isolation.
- The FPGA can generate its own pseudo-random data pattern (2^{23}-1), which is output via the TLK2711 transmit path and looped back to the receiving side (either via internal loopback mode or an external cable). The FPGA will verify the received data pattern and report any errors.

The SERDES TX clock is 125 MHz with a 50% duty cycle. It is generated by an oscillator local to the SPM. It routes to the FPGA as well as both TLK2711 SERDES transceivers as the GTX_CLK input. The TLK2711 has a rather tight jitter requirement (40 ps peak-to-peak) and the oscillator was chosen to meet that requirement. This clock is used inside the FPGA to clock out the SERDES transmit data (TXD[15:0]) to either TLK2711 transceiver for loop-back test modes.

When a serial data stream is received by either TLK2711 transceiver, it recovers and outputs a RX clock along with the SERDES receive data (RXD[15:0]) and K-code indicator signals (RKLSB and RKMSB). The RX clock is used inside the FPGA to clock in the receive data and also used to drive the logic for the sync pattern, decode error, PRBS error, and loss-of-signal (LOS) detection on the TLK2711 receive signal. The data is synchronized over to the primary FPGA clock domain (TCXO clock) via a dual-clock FIFO buffer.

LDPC Encoder—This core consists of an encoder for the CCSDS-standard LDPC code of rate 7/8 (often referred to as code C2), followed by a pseudo-randomizer, and a circuit to insert Attached Synchronization Markers (ASMs) prior to each codeword, as shown in Figure 7.

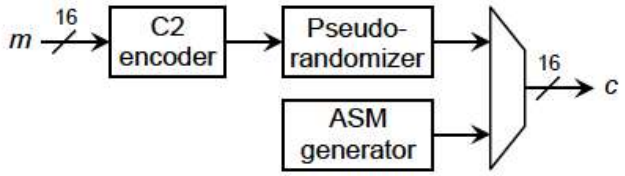

Figure 7 - LDPC Encoder Functional Block Diagram

The encoder takes k = 7136 input bits as a series of 446 16-bit words. It generates 32 ASM symbols followed by n = 8160 encoded and pseudo-randomized output symbols, as a series of 512 16-bit words. The first word of an input message must be indicated by setting the start-of-frame input high. The first word of the generated ASM is marked by the start-of-frame output, and the last word of the codeword is marked by the end-of-frame output.

OQPSK Modulator—The output of the encoder module is modulated using Offset Quadrature Phase-Shift Keying (OQPSK). The modulation is performed on 16-bits at a time in parallel and takes into account the data rate, with 2 complex samples per channel symbol at 2 Gbps, 4 complex samples per channel symbol at 1 Gbps, and 8 complex samples per channel symbol at 500 Mbps.

Pulse Shaping Filter—In order to reduce intersymbol interference (ISI) and reduce the bandwidth of the modulated signal a pulse-shaping root-raised-cosine (RRC) filter is included between the OQPSK modulator and the DAC interface. It can optionally be selected or bypassed.

Given that the data in the MP is processed in 16-bit parallel words, a parallel RRC filter implementation is required, as 16 results per each I and Q channel need to be calculated in a single clock cycle. The filter design includes a set of programmable coefficients to allow for a real-time reconfiguration and added flexibility. In this implementation, the parallel symbols from the modulator are registered and a windowing function is used to select the coefficients stored in the MP FPGA registers. The 16-bit I and Q filter outputs are then routed to the DAC interface logic.

Digital to Analog Converter Interface—The MP FPGA interfaces to two E2V EV12DS130AG DACs, one for the in-phase symbol component and one for the quadrature symbol components. The DACs output analog samples at 2 Gsps, which is too fast for the FPGA to operate. To allow the FPGA to operate at a reasonable speed and still provide data at 2 Gsps, the DACs incorporate a built-in 4:1 multiplexer (MUX) so that the FPGA outputs four 12-bit samples in parallel at 500 MHz (250 MHz DDR).

The FPGA outputs the DAC samples at 500 MHz, but that is still a very fast rate to run the logic inside the FPGA fabric. To enable the internal logic to run even slower, the OSERDES blocks in the Virtex-5 Input-Output Blocks (IOBs) are utilized to provide another level of 4:1 MUX. This allows the logic to run at 125 MHz, with only the hard-coded OSERDES blocks running at 500 MHz (250 MHz DDR). In this way, each of the two FPGA DAC interface modules receive 16 samples in parallel from the modulator module (125 MHz), which are then muxed down to 4 samples in parallel in the OSERDES blocks (500 MHz) and then down again to a single sample at a time inside the DACs themselves (2 GHz).

Each of the two DACs (DAC-I and DAC-Q) receives the same 2 GHz clock from the KTM and generates its own 250 MHz (DDR) clock that is provided to the FPGA to be used to clock out data to the respective DAC.

Inside the FPGA, the data enters from a single source (the SSR via the SERDES link) and is split into I and Q components in the modulator module. It is critically important that the I and Q components stay in clock cycle alignment with each other. If the I and Q components were synchronized over to separate clock domains before being clocked out to the DACs, clock cycle alignment could not be guaranteed (due to the unpredictable nature of metastable flip-flop outputs). To avoid this problem, both I and Q components are clocked out to the DACs using a single clock domain (DAC-I clock), which is acceptable from a timing perspective because the DAC-Q clock is almost identical to the DAC-I clock (only difference being due to process variations between the DACs). The modulator output data is synchronized from the primary FPGA clock domain (TCXO clock) via a dual-clock FIFO buffer.

Software Overview—The Space Telecommunications Radio

System (STRS) architecture for software defined radios provides a common, consistent framework for hardware abstraction of complex reconfigurable and reprogrammable radio systems. The standard calls for generalized and modular hardware designs, and provides an open architecture design to accommodate the various mission-specific needs envisioned by NASA missions. The UST-KaM software is primarily developed in accordance with a software management plan that adheres to the STRS platform.

The UST-KaM uses two main modes of software operation, transitioned by commands or resets to the unit. Figure 8 provides a simplified software mode transition diagram. In a reset or power-on condition, the Boot Code Software (BCSW) is loaded to the SPARC processor from the on-board one-time programmable PROM, and the UST-KaM is brought to a pre-defined safe state. The BCSW is an interrupt-based, single-threaded application that interacts directly with the hardware peripheral devices in order to provide full command and control of the unit, collect and report engineering telemetry for health and safety, configure and program the signal processing hardware, and also performs built-in self-tests for debugging and troubleshooting purposes. It is in this mode that the software and signal processing functions (outside the context of the BCSW) can be reconfigured and reprogrammed to provide post-launch in-flight changes to the UST-KaM. Operating out of the PROM is also commonly referred as the Safe Mode. In case of a fault, the Safe Mode could be used as a recovery console to reprogram or correct the configuration of the DPM as necessary.

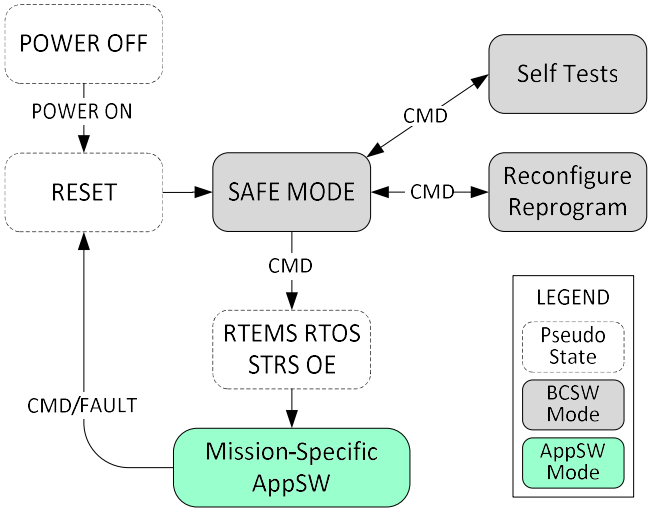

Figure 8 - UST-KaM Software Mode Transition Diagram

The BCSW developed for the UST-KaM is baselined from various successful JPL flight radio designs such as the Electra units for MRO/MAVEN, the CoNNeCT SDR as part of NASA's Space Communications and Navigation (SCaN) testbed, as well as the Digital Electronics Assembly of the Terminal Descent Sensor of the Mars Science Laboratory. Commands supplied via the 1553 bus interface allow the UST-KaM to transition to an STRS Application Software (AppSW) mode, where mission-specific signal processing needs can be loaded and executed.

In the STRS AppSW mode, the POSIX-compliant application layer specific to the UST-KaM is executed on top of the STRS Operating Environment (OE). For example, the AppSW for the UST-KaM is capable of configuring the encoding and modulation parameters to the desired data rates, channel coding types, and modulation schemes. The STRS OE provides standardized multi-platform features through Application Program Interfaces (APIs) that initialize and configure the hardware platform as well as provide controls for file/memory handling. An Operating System (OS) is also an integral part of the STRS OE, and the Real-Time Executive for Multiprocessor Systems (RTEMS) Real-Time OS is built to provide the fast, low overhead context switching and deterministic scheduling mechanism.

The developed software codes are mostly written in C/C++ with some assembly code. The code base is also highly memory efficient, and current memory utilization margins are over 90%, which allows for greater expansion capabilities and easier code upgrades.

Ka-band Transmit Module (KTM)

The Ka-band Transmit module (KTM) is a multifunction module composed of a Ka-band heterodyne up-converter, a 2 GHz phase-locked loop (PLL) frequency synthesizer, and a 125 MHz PLL frequency synthesizer. A block diagram of the KTM is shown in Figure 9.

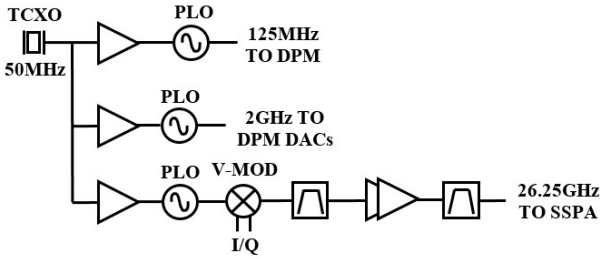

Figure 9 - KTM Multi-Function Module Block Diagram

The reference input of the KTM is fed by a low phase noise Temperature Compensated Crystal Oscillator (TCXO) located in the Frequency Reference Module (FRM). The three PLL synthesizers in the KTM are phase locked to this TCXO input. The 125 MHz PLL synthesizer feeds the digital processor module (DPM) clock input and is used as a back-up relatively stable low phase noise source for FPGA processing. The 2 GHz PLL synthesizer is used to clock the digital-to-analog converters (DACs) located in the DPM. The Ka-band converter electronics in the KTM is composed of a Ku-band (13.125 GHz) PLL synthesizer which provides the Local Oscillator (LO) tone for the sub-harmonic IQ

mixer. The IQ mixer is used to modulate the in-phase (I) and quadrature (Q) digital waveforms onto the second harmonic of the LO input. Early on in the architectural trade study, prototypes of various modulators were characterized to determine which modulator was best suited for this application. In the end the subharmonic IQ mixer was selected. One benefit of the sub-harmonic mixer is that it eliminates the need for a higher frequency local oscillator that would require a Ka-Band VCO. The candidate flight Ka-band VCOs had degraded efficiency and phase noise even when including the 20logN phase noise hit compared to that of the Ku-band MMIC VCO selected. Following the subharmonic IQ mixer are clean-up Ka-band bandpass filters and driver amplifiers used to provide the input of the external solid-state power amplifier (SSPA) with a signal of sufficient drive level.

Architecture RF Simulation—As part of the architectural evaluation, a system simulation was performed in Applied Wave Research (AWR) Virtual System Simulator (VSS). The constellation and spectrum results are shown in Figure 10 and Figure 11 for the modulator simulation with a 2 Gbps QPSK digital waveform on the I and Q inputs.

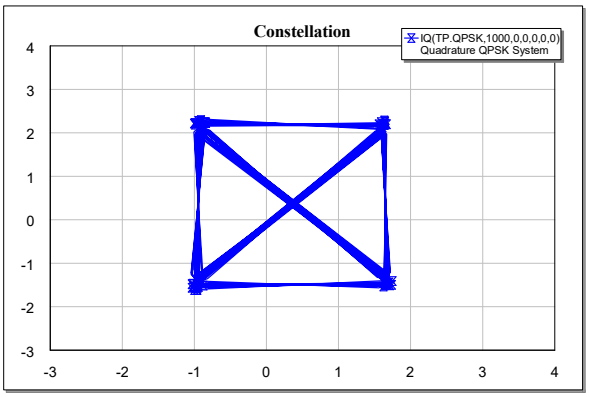

Figure 10 - AWR VSS Constellation Results of Architecture in QPSK Simulator Bench

Hardware—All of the components in the KTM were selected in order meet the reliability, radiation and RF performance requirements set forth by the NISAR program. In addition to this, the design of any modules belonging to the UST platform are capable of meeting most deep space applications. For example, the components are selected to withstand a total ionizing dose (TID) of at least 100 kRad (Si) and are single event effect (SEE) tolerant. All parts are capable of being screened to Class S space level when applicable.

In addition to the parts reliability, the printed circuit board (PCB) assembly packaging approach prioritized the overall reliability of the KTM assembly. For example, exposed chip and wire assemblies were avoided at the PCB top assembly level to ease the handling and foreign object debris (FOD) requirements. With the exception of the custom Quartz RF filters and grounded coplanar waveguide transition, all components utilize standard Surface Mount Technology (SMT) assembly processes.

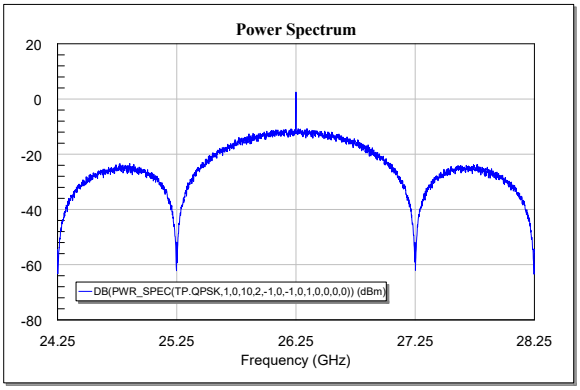

Figure 11 - AWR VSS Spectrum Results of Architecture in QPSK Simulator Bench

In order to realize an all SMT approach for the active components, custom high frequency leadless chip carrier (LCC) modules from KCB Solutions were used [4]. One example of this was the subharmonic IQ modulator in which a multichip module (MCM) was designed by KCB. This MCM LCC contains the sub-harmonic IQ mixer, LO amplifier and RF amplifier MMICs in an SMT hermetic package shown in Figure 12.

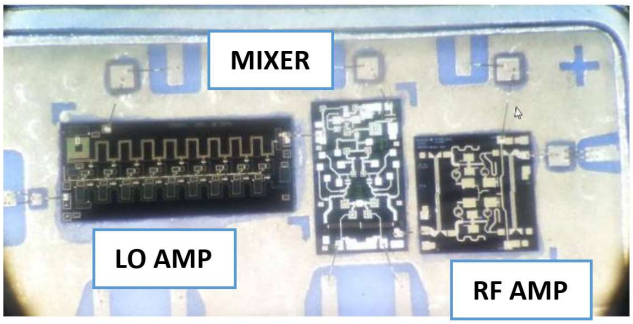

Figure 12 - De-lidded Modulator MCM in Custom High Reliability Hermetic Ceramic Package

The corresponding fully assembled test board for this MCM is shown in Figure 13. The modules are all tested prior to assembly at the PCB level on a fixture similar to that shown in the figure.

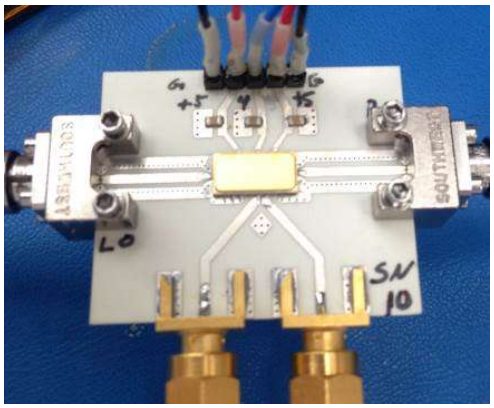

Figure 13 - SMT Packaged High Rate Modulator on Custom Evaluation Board

The top level printed wiring assembly (PWA) contains all of the active electronic components in the KTM. Figure 14 and Figure 15 show photos of the top and bottom of the printed wiring assembly prior to attaching it into the chassis.

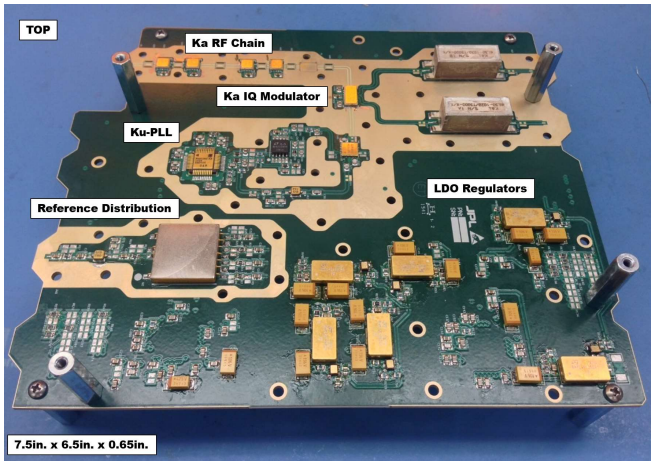

Figure 14 - KTM PWA Top Side

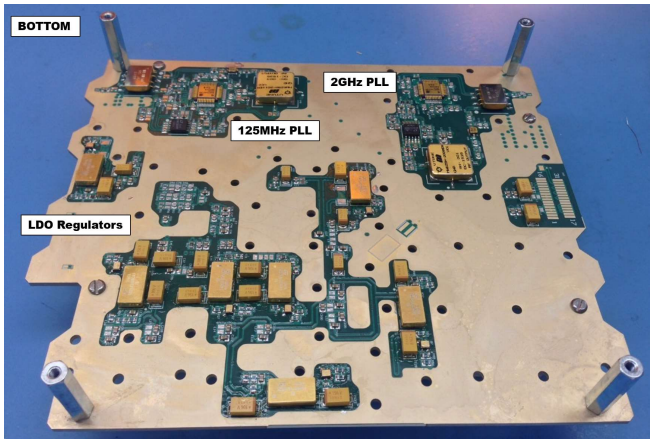

Figure 15 - KTM PWA Bottom Side

The top of the PCB houses the Ka-Band electronics, the reference distribution circuitry and power conditioning for the bottom side electronics. On the backside of the PCB are the 125 MHz and 2 GHz PLLs along with the top side power conditioning electronics.

In order to decrease crosstalk amongst the various circuits, the internal floor of the chassis is pocketed to help isolate circuits based on their functionality and noise sensitivity. In addition to the internal floor pockets, two clamshell covers are also used to isolate the circuitry on the top side of the PCB. Figure 16 and Figure 17 show the top and bottom of the fully assembled KTM with no external lids.

Figure 16 - KTM Slice Top View

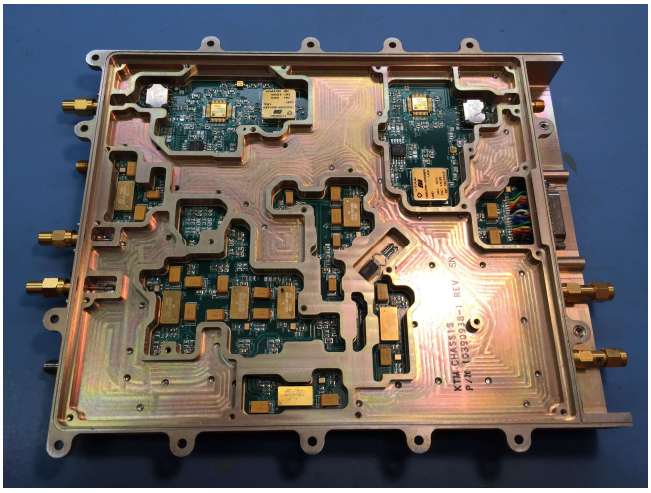

Figure 17 - KTM Slice Bottom View

Power Supply Module (PSM)

The PSM provides secondary post-regulated DC power to the other modules of the UST-KaM as well as distributes the main frequency reference signal. The PSM was originally designed to provide additional secondary voltages to support a variety of UST configurations [3]. The PSM for the UST-KaM uses the same overall architecture, electronic parts, hardware layout, and thermal design, but with unneeded converters and circuitry left unpopulated. The simplified block diagram of the UST-KaM PSM is shown in Figure 18, and the assembled module is shown in Figure 19.

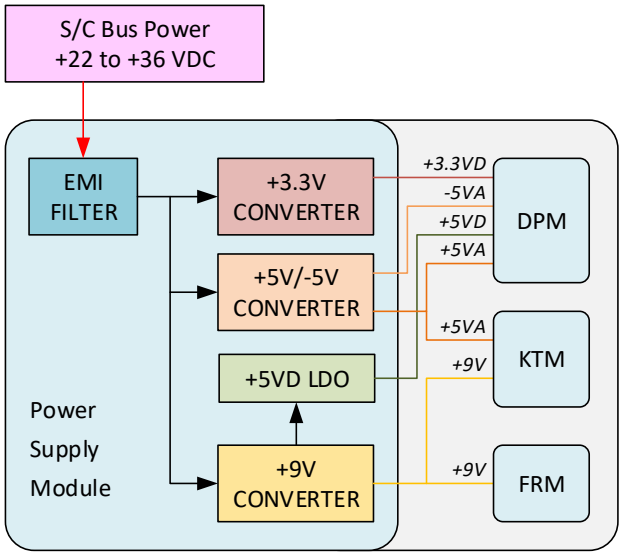

Figure 18 - UST-KaM PSM Block Diagram

The Frequency Reference Module (FRM) is a sub-module that resides in an RF isolated cavity in the PSM chassis. It utilizes high reliability, radiation hardened components, including a 50 MHz temperature compensated crystal oscillator (TCXO). The 50 MHz signal is divided and provided to the other modules as a common reference for phase locking purposes.

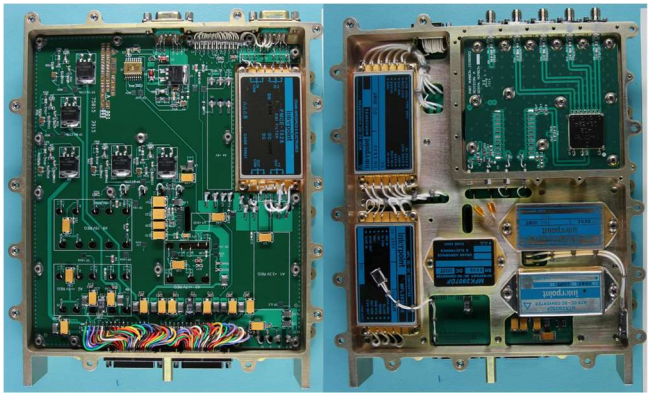

Figure 19 - Power Supply Module Slice

4. Test Results

NASA technology readiness level (TRL) 6 is achieved on the UST-KaM Engineering Model (EM) through rigorous functional and performance testing in a relevant environment in preparation for the NISAR mission. Three-axis dynamics, thermal vacuum, and EMI/EMC testing were all performed at the JPL Environmental Test Lab. The UST-KaM's RF performance, including carrier phase noise, error vector magnitude (EVM), output power, and spectral emissions, were characterized over temperature, in addition to standard parameters such as DC power consumption. Compatibility was demonstrated against two commercially-available ground-station receivers capable of up to 2 Gbps: a ViaSat VHR-3200 High-Rate Modem [6], and a Zodiac Cortex High Data Rate Receiver [7]. Furthermore, a vendor-provided Output Validation Unit (OVU) was used to verify the SSR WizardLink (WzL) interface to show end-to-end data flow integrity through the UST-KaM.

Figure 20 shows the basic test setup for the UST-KaM. AOS Transfer Frames are generated in the SSR OVU and transferred to the UST-KaM via the flow-controlled WzL interface. The AOS Transfer Frames are LDPC encoded and the Attached Sync Marker (ASM) is prepended, and modulated to a Ka-band output in the UST-KaM. The RF waveform is down-converted to a suitable intermediate frequency (IF) before it is demodulated in the high-rate receiver. For performance tests, the SSR OVU provides a pseudorandom binary sequence (PRBS-23) that the high-rate receivers analyze and provides the bit-error rate (BER).

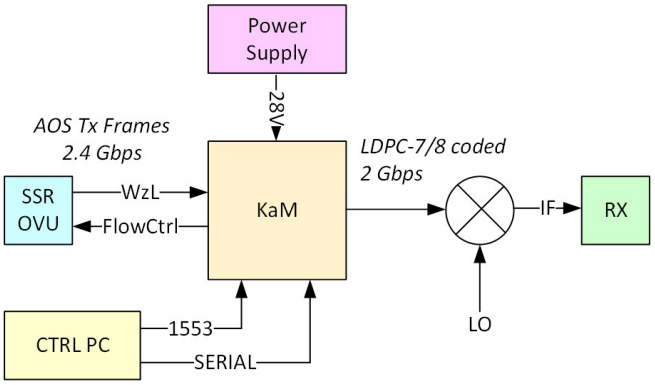

Figure 20 - UST-KaM Test Setup

Table 2 - UST-KaM EM Measured Performance

Parameter	Units	Spec.	Meas.
DC Power Consumption (Transmit Mode)	Watts	< 50.0	40.9
DC Power Consumption (Standby Mode)	Watts	< 24.0	19.9
RF Output Power	dBm	> 12.0	12.4
Carrier Frequency	GHz	26.25	26.25
Carrier Phase Noise (1 kHz – 10 MHz)	deg, rms	< 3.6	3.1
Coded Data Rate	Gbps	2.0	2.0
Phase Imbalance	deg	< 5.2	3.5
Amplitude Imbalance	dB	< 1.1	0.4
Spurious Outputs	dBc	< -60	None

Table 2 summarizes the key, worst-case performance values measured on the EM unit. The measurements are all well within the required specification limits for the NISAR mission. Figure 21 shows the measured BER performance curve and the constellation diagram at 2 Gbps. The measurement shows an implementation loss of approximately 1 dB at 1E-8 BER.

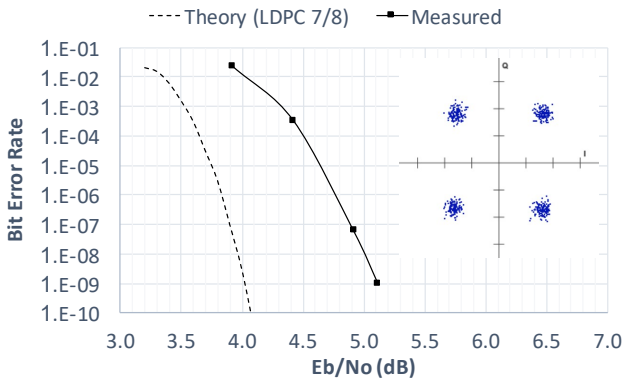

Figure 21 - Measured BER Curve and Constellation Diagram at 2 Gbps

Figure 22 shows the measured spectrum output from the UST-KaM, as well as the spectrum output passed through a representative power amplifier operating at the 1 dB compression point. Approximately 10 dB of spectral regrowth is observed through the amplifier, which is consistent with the previous simulations. Given NISAR plans to occupy the full 1500 MHz allocated bandwidth of the Earth Exploration Satellite Service band (25.5 to 27.0 GHz), an output waveguide bandpass filter is also planned to help ensure spectral compliance with the NTIA.

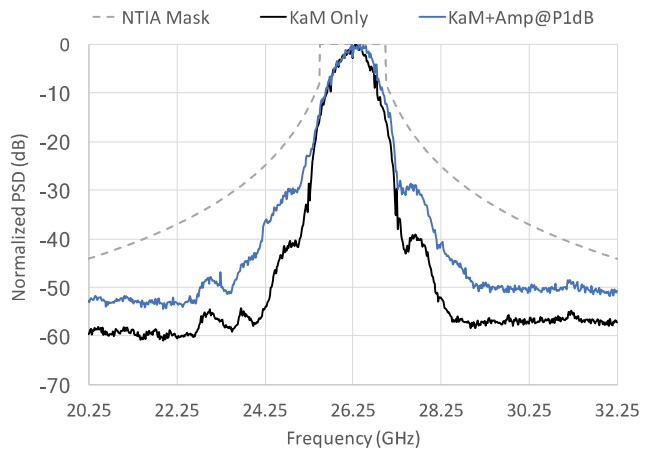

Figure 22 - Measured Output Spectrum

Additional testing with digital pulse-shaping demonstrated the UST-KaM is capable of transmitting with a more confined spectrum in mission scenarios without a compressed RF amplifier. Figure 23 shows the measured spectrum using a Root Raised Cosine (RRC) digital filter with an 8 symbol span and 2 samples per symbol. RRC rolloff factors of 0.6 and 0.4 were measured, and both produced the expected spectral outputs.

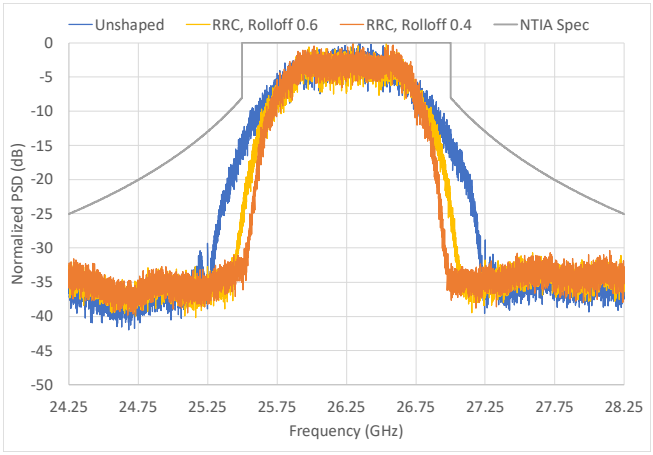

Figure 23 - Measured Transmit Spectrum with Pulse Shaping

5. CONCLUSIONS & FUTURE PLANS

NISAR Flight Plans

The NISAR project is currently in the flight hardware build phase with a scheduled launch for late 2020. Three flight models of the UST-KaM are currently being assembled, with two planned to be integrated on the spacecraft and one available as a flight spare. These flight models will be integrated in 2018 and complete a proto-flight qualification program in 2019.

The NISAR Ka-band telecom subsystem (shown in Figure 24) consists of both JPL and ISRO provided hardware, including a separate Ka-band transmitter that will downlink to ISRO ground stations. The UST-KaM units will each connect to external SSPAs, followed by waveguide filters to help reject undesired out-of-band spectral emissions and protect nearby frequency bands used for radio science. Both the JPL and ISRO transmitters will share a gimbaled 70 cm high-gain antenna. For UST-KaM downlinks, current proposed NASA antenna complexes are located in Alaska (USA), Svalbard (Norway), Punta Arenas (Chile), and TrollSat (Antarctica).

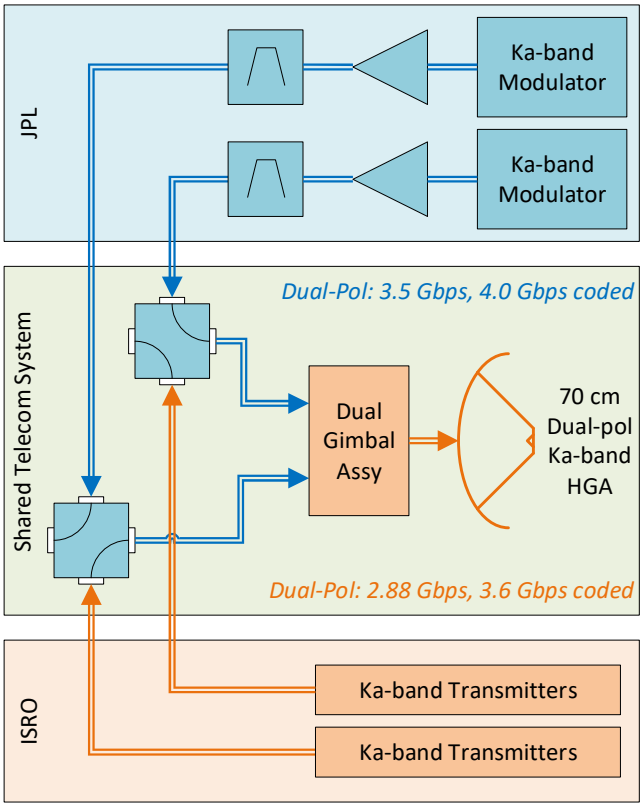

Figure 24 - NISAR Ka-band Telecom Subsystem

Future Plans

Since they are first-time flight builds, the UST-KaM units for NISAR are being built and tested at JPL. However, for additional builds needed for future mission, JPL will likely select and work with an industry partner better equipment to handle the assembly and testing of more units. This approach is consistent with pervious JPL radio developments, such as the Electra UHF transceivers used for relay communications at Mars, where JPL has collaborated with an industry partner to provide radios for five separate Mars mission.

Additional research and development is also planned for the UST-KaM. For certain mission scenarios with sufficient link SNR and linear amplification, JPL is investigating a higher data rate mode of operation. Utilizing two SERDES inputs simultaneously and 16-APSK modulation with RRC pulse shaping, a single UST-KaM could support up to ~4.1 Gbps transmission rate. This could allow mission using dual polarization to reach data downlink rates greater than 8 Gbps.

6. References

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Biographies

Michael Pugh *received his M.S. in Electrical Engineering from University of Southern California and his B.S. from Harvey Mudd College. He has been with NASA's Jet Propulsion Laboratory since 2007 where he is currently the supervisor for the Communications System Engineering group. He is the Cognizant Engineer for the Universal Space Transponder, including the UST-KaM for the NISAR mission. He previously served as System Engineer for the ExoMars TGO Electra payload.*

Igor Kuperman *is the supervisor of the Spacecraft Reconfigurable Communication Systems group at the Jet Propulsion Laboratory and has over 15 years of experience ranging from digital signal processing (DSP) design and analysis to FPGA development and implementation of DSP, coding, and other data processing algorithms. Mr. Kuperman received his M.S. from University of Southern California in 2005 and his B.S. from California State Polytechnic University, Pomona, in 2001, both in Electrical Engineering. Recently, he was the cognizant engineer for the digital subsystem of the MSL landing radar as well as the FPGA lead for the latest Electra UHF radio firmware deliveries for the MRO and MSL projects. Mr. Kuperman is currently serving as the Product Delivery Manager for the ExoMars Trace Gas Orbiter Electra communication subsystem and as the Task Manager for the Universal Space Transponder EM development.*

M. Michael Kobayashi *received his B.S. (2006) and M.S. (2007) in Electrical Engineering from UC Irvine, and joined the Jet Propulsion Laboratory in 2007 as an RF Microwave Engineer. He has worked on various microwave flight hardware deliveries to MSL and SMAP, and has been involved in developing the*

Iris Deep-Space Transponder software-defined radio to support various JPL CubeSat projects such as INSPIRE, MarCO, and Lunar Flashlight. Recently, he has been involved in developing the digital slice of the UST, and system engineering for NISAR.

Fernando Aguirre *received a B.S. (2002) and an M.S. (2007) in Electrical Engineering from UCLA. He has been with NASA's Jet Propulsion Laboratory since 2008 where he is a microwave design engineer in the Spacecraft Reconfigurable Communication Systems group. He has worked on hardware for various JPL flight and research projects. Most recently he is the RF design engineer for the UST exciter modules and the Frequency Reference Module. Prior to joining JPL he was a microwave engineer at REMEC Defense and Space where he designed microwave synthesizers and amplifiers for military applications.*

Michael Kilzer *received his B.S. (2011) and M.S. (2013) in Electrical Engineering from Cornell University in Ithaca, NY. He joined the Jet Propulsion Laboratory in 2013 as an Electrical Engineer in the Tracking Systems and Applications section. At JPL, he has been involved in FPGA development for multiple projects, such as the GRACE-FO Laser Ranging Instrument, MarCO, and UST MP-KaM EM. In addition to FPGA engineer, he is system engineer for the SWOT GPSP and Sentinel-6 GNSS-RO instruments, and currently FPGA engineer for the CoNNeCT VCM/ACM task and NISAR MP-KaM FPGA.*

Carl Spurgers *received his B.S. and M.S. in Electrical Engineering from the University of Texas at Dallas with a focus in RF and microwave design. Prior to JPL, he supported digital and RF hardware design efforts for several military applications while at Rockwell Collins and L-3 Communications, including conformal composite UHF phased array antennas. He arrived at JPL in 2013 and has since supported a variety of programs including NISAR, SWOT, DSOC, FINDER, Mars ADT, Mars 2020 Rover, and Mars Helicopter Scout. Assignments include design of digital electronics for the NISAR UST-KaM radio, capable of downlinking data to earth over Ka-Band at 1 Gsps OQPSK, and piezoelectric transducer amplifier and receiver electronics for use in an acoustic modem to support down-hole wireless communications.*

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